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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/510,659	06/09/2005	Thomas Fuehrer	10194/3839	9228

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KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

EXAMINER

JAHANGIR, KABIR U

ART UNIT	PAPER NUMBER
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2168

MAIL DATE	DELIVERY MODE
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02/07/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/510,659

Applicant(s)

FUEHRER ET AL.

Examiner

Kabir Jahangir

Art Unit

2168

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 November 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 6-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 6-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application
- ☐ Other: _____

DETAILED ACTION

1. This Action is responsive to the applicants' argument filed on November 12, 2007. Please note claims 6-13 are pending.

Response to Arguments

2. Applicants' arguments filed on November 12, 2007 with respect to claims 6-13 have been fully considered but are not persuasive.

In response to applicants' argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

First of all, pages 2-4 concerning claim 6, applicants' argued that there is no suggestion or motivation to combine the Devore and Banister references. However, Examiner respectfully submits that Devore and Banister both references concern about data transmission which is the same field of endeavor as applicants' invention. Furthermore, Devore and Banister have been combined to enhance error control (see col. 2 lines 35-39 of Devore).

Second of all, Concerning claims 7-8 and 10-13, Applicant presents an argument similar to what applicable to claim 6. Examiner respectfully applies a same similar response as previously described.

Finally, at page 5 concerning claim 9, applicants' argued that there is no suggestion or motivation to combine the Devore, Banister and Padovani references. However, Examiner respectfully submits that Devore, Banister and Padovani references concern about data transmission which is the same field of endeavor as applicants' invention. Furthermore, Devore, Banister and Padovani have been combined to optimize the efficiency of data communication (see paragraph [0009] of Padovani).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 6-8 and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Devore et al. (US Patent 3821703, hereafter "Devore") in view Banister et al. (US Patent 6567390, hereafter "Banister").

Devore and Banister are analogous art because they are from the same field of endeavor of data transmission.

As per claim 6, Devore discloses a method for padding segments for transmitting data on a bus system, the segments having a preset total number of binary information pieces, comprising:

"transmitting the data in the segments" (see col. 2 lines 35-39 wherein transferring signal data which is equivalent to 'transmitting the data in the segments'); and

"in the event of transmission of data including less binary information than a predetermined total number of the segments, padding the total number of the segments by a filling pattern of a corresponding number of binary information pieces (see col. 2 lines 55-63 wherein padding the segment which is equivalent to 'padding the total number of the segments' to make a full segment which is equivalent to 'total number of the segments' when there are less number of bits which is equivalent to 'less binary information'),

"wherein the filling pattern includes a number of binary information pieces that corresponds to the total number of the segments" (see col. 2 lines 55-63 wherein padding the bit sufficient enough which is equivalent to 'filling pattern includes a number of binary information pieces' to make a full segment which is equivalent to 'total number of the segments').

However, Devore does not disclose that padding data are first written into the segment, and wherein the binary information of the data is subsequently written into the same segment, the particular binary information of the filling pattern being overwritten by the binary information of the data.

Banister discloses that padding data are first written into the segment, and wherein the binary information of the data is subsequently written into the same segment, the particular binary information of the filling pattern being overwritten by the binary information of the data (see col. 7 lines 15-28 wherein first initializing the frame with padding bits which is equivalent to 'padding data are first written into the segment' then overwriting with the actual data which is equivalent to 'filling pattern being overwritten by the binary information of the data').

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the initialization of padding bits first, then overwriting

with the actual data of Banister with Devore because it would help to enhance error control (see col. 2 lines 35-39 of Devore).

As per claim 7, as set forth in claim 6, Devore and Banister as combined and furthermore Devore discloses that binary information pieces include bytes (see Abstract and col. 4 lines 55-67 wherein signal data are in bytes).

As per claim 8, as set forth in claim 6, Devore and Banister as combined and furthermore Devore discloses the binary information of the filling pattern and the binary information of the data are written in a buffer memory into the segment, and the segment is transmitted from the buffer memory to the bus system (see col. 2 lines 62-68 and col. 3 lines 1-2 wherein data are processed in buffer system).

As per claim 10, Devore discloses a device for padding segments for transmitting data on a bus system, the segments having a predetermined total number of binary information pieces, comprising:

“a first arrangement for transmitting the data in the segments” (see col. 2 lines 35-39 wherein transferring signal data which is equivalent to ‘transmitting the data in the segments’); and

“a second arrangement for, in the event of transmission of data including less binary information than the predetermined total number of the segment, padding the total number of the segment through a filling pattern of a corresponding number of binary information pieces” (see col. 2 lines 55-63 wherein padding the segment which is equivalent to ‘padding the total number of the segments’ to make a full segment which is equivalent to ‘total number of the segments’ when there are less number of bits which is equivalent to ‘less binary information’),

“wherein the second means first writes the filling pattern, whose number of binary information pieces corresponds to the total number of the Segment, into the segment” (see col. 2 lines 55-63 wherein padding the bit sufficient enough which is equivalent to ‘filling pattern includes a number of binary information pieces’ to make a full segment which is equivalent to ‘total number of the segments’).

However, Devore does not disclose that padding data are first written into the segment, and wherein the binary information of the data is subsequently written into the same segment, the particular binary information of the filling pattern being overwritten by the binary information of the data.

Banister discloses that padding data are first written into the segment, and wherein the binary information of the data is subsequently written into the same segment, the particular binary information of the filling pattern being overwritten by the binary

information of the data (see col. 7 lines 15-28 wherein first initializing the frame with padding bits which is equivalent to 'padding data are first written into the segment' then overwriting with the actual data which is equivalent to 'filling pattern being overwritten by the binary information of the data').

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the initialization of padding bits first, then overwriting with the actual data of Banister with Devore because it would help to enhance error control (see col. 2 lines 35-39 of Devore).

As per claim 11, as set forth in claim 10, Devore and Banister as combined and furthermore Devore discloses that binary information pieces include bytes (see Abstract and col. 4 lines 55-67 wherein signal data are in bytes).

As per claim 12, Devore discloses a bus system, comprising: a device for padding segments for transmitting data on the bus system, the segments having a predetermined total number of binary information pieces, the device including:

"a first arrangement for transmitting the data in the segments" (see col. 2 lines 35-39 wherein transferring signal data which is equivalent to 'transmitting the data in the segments'); and

“a second arrangement for, in the event of transmission of data including less binary information than the predetermined total number of the segment, padding the data to the total number of the segment through a filling pattern of a corresponding number of binary information pieces” (see col. 2 lines 55-63 wherein padding the segment which is equivalent to ‘padding the total number of the segments’ to make a full segment which is equivalent to ‘total number of the segments’ when there are less number of bits which is equivalent to ‘less binary information’),

“wherein the second means first writes the filling pattern, whose number of binary information pieces corresponds to the total number of the segment” (see col. 2 lines 55-63 wherein padding the bit sufficient enough which is equivalent to ‘filling pattern includes a number of binary information pieces’ to make a full segment which is equivalent to ‘total number of the segments’).

However, Devore does not disclose that padding data are first written into the segment, and wherein the binary information of the data is subsequently written into the same segment, the particular binary information of the filling pattern being overwritten by the binary information of the data.

Banister discloses that padding data are first written into the segment, and wherein the binary information of the data is subsequently written into the same segment, the particular binary information of the filling pattern being overwritten by the binary

information of the data (see col. 7 lines 15-28 wherein first initializing the frame with padding bits which is equivalent to 'padding data are first written into the segment' then overwriting with the actual data which is equivalent to 'filling pattern being overwritten by the binary information of the data').

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the initialization of padding bits first, then overwriting with the actual data of Banister with Devore because it would help to enhance error control (see col. 2 lines 35-39 of Devore).

As per claim 13, as set forth in claim 12, Devore and Banister as combined and furthermore Devore discloses that binary information pieces include bytes (see Abstract and col. 4 lines 55-67 wherein signal data are in bytes).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Devore et al. (US Patent 3821703, hereafter "Devore") in view Banister et al. (US Patent 6567390, hereafter "Banister") as applied to claim 6 above, and further in view of Padovani et al. (US Patent Application 2003/0063583, hereafter "Padovani").

Devore, Banister and Padovani are analogous art because they are from the same field of endeavor of data transmission.

As per claim 9, Devore and Banister as combined disclose padding segments for transmitting data in a bus system.

However, does not disclose that the bus system is a time-controlled bus system, and the segments correspond to time slots on the bus system, the data being transmitted in the corresponding time slots.

Padovani discloses that the bus system is a time-controlled bus system, and the segments correspond to time slots on the bus system, the data being transmitted in the corresponding time slots (see process the data packet over a time slot, in paragraph [0020]).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the time controlled bus system of Padovani with Devore and Banister because it would help to optimize the efficiency of data communication (see paragraph [0009] of Padovani).

Conclusion

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kabir Jahangir whose telephone number is 571-270-1761. The examiner can normally be reached on Mon-Fri, 9:00am-5:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Vo can be reached on 571-272-3642. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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K)
KJ

Patent Examiner

January 24, 2008


TIM VO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

